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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	09/899,573	ERRATICO, PIETRO	
	Examiner	**Art Unit**	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) *27-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/19/03 has been entered as Paper No. 18.

Response to Amendment

Amendment C filed 04/28/03 has been entered as Paper No. 16, in view of the Request for Continued Examination of Paper No. 18. In Amendment C Applicant substantially amended claims 12, 17 and 22 (i.e., all elected independent claims). Comments on Remarks by Applicant in said Amendment C are included below under "Response to Arguments".

Response to Arguments

The rejection based on Boden Jr. could not be maintained after Amendment B because the second region by Boden is either connected to the same electrode as the first region or one of said first and second regions is not necessarily taught to be under the influence of any electrode capable of biasing (see column 3 in Boden Jr.). A new search has revealed grounds for rejections of all non-canceled, elected claims 12-26. Furthermore, the examiner draws attention to the double patenting issue concerning claim 19 (see "Double Patenting").

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claim 12-13 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE Journal of Solid-State Circuits, Vol. SC-20 (1), February 1985).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines 21-63) positioned on one side of said first region and extending from the surface of said epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 comprising a dielectric material 38 (cf. col. 3, lines 37-44) adjacent

said epi layer and polycrystalline silicon 42 (cf. col. 3, lines 55-62) spaced apart from said epi layer by said dielectric material, said isolating element also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al do not necessarily teach the second region as claimed. However, the purpose of the isolation trench by Hunter et al has clearly been stated to include trench isolation for suppressing latch-up in CMOS devices (cf. col. 1, lines 12-28); therefore, an obvious application of the isolation trench by Hunter et al is to the CMOS device structure of Figure 1 in Yamaguchi et al in which the central trench separates NMOS and PMOS devices, the NMOS device being on the side of the said first region, while the second region is the N+ region biased, in fact: connected, to Vss, while said first region is biased by the gate electrode of the PMOS device. Hence it is seen that the not specifically claimed limitations by Hunter et al are present in an obvious application of the kind for which Hunter et al intended their trench isolation invention.

Motivation to include said teaching by Yamaguchi et al is provided by the intended application by Hunter et al to deep trench isolation of CMOS devices (inter alia) as stated in their "Background", for the purpose of latch-up suppression (cf. col. 1, line 24). *Combination* of said teaching with said invention is straightforward because at most the trench already shown by Yamaguchi et al would have to dug a little more deeply into the P+ substrate. *Success* of the implementation of said combination can therefore be reasonably expected.

On claim 13: in the device of claim 12 as essentially taught by Hunter et al and Yamaguchi et al the isolating element at least partially surrounds said first region (cf.

Figure 1 in Yamaguchi et al) which obviously increases improvement of the latch-up protection.

On claim 15: in the device by Hunter et al and Yamaguchi et al the first conductivity type is p-type (see discussion of claim 1).

4. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al and Yamaguchi et al as applied to claim 12 above, and further in view of Nakagawa (6,239465 B1).

As detailed above, Claim 12 is unpatentable over Hunter et al and Yamaguchi et al, who do not necessarily teach the further limitation as defined by claim 14. However, Nakagawa teaches isolation trenches for prevention of electrical interference between different portions of the device and with a length substantially equal to the width of the chip (cf. Figures 5 and 8).

Motivation to include the teaching by Nakagawa in the invention of Hunter et al and Yamaguchi et al is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in Hunter et al and Yamaguchi et al not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Hunter et al and Yamaguchi et al in accordance with the abovementioned

teaching by Nakagawa so as to accentuate the role and function of the isolation element as essentially taught by Hunter et al and Yamaguchi et al.

5. ***Claim 16*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al and Yamaguchi et al as applied to claim 12 above, and further in view of Mavencamp (6,175,277). Although Hunter et al and Yamaguchi do not necessarily teach the further limitation as defined by claim 16, application of the device by Hunter et al and Yamaguchi et al, i.e., a CMOS device with latchup protection, to power transistors is an obvious application of the invention, as evidenced from Mavencamp, who teaches CMOS power transistors (see, for instance, claim 1 by Mavencamp), while it is understood in the art that latchup is a ubiquitous concern for CMOS devices. Claim 16 thus merely recites an obvious application of the invention.

6. ***Claim 17-20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE Journal of Solid-State Circuits, Vol. SC-20 (1), February 1985).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines 21-63) positioned on one side of said first region and extending from the surface of said

epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 at least partially surrounding said first region 12 (cf. Figure 2), said isolating element also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al do not necessarily teach the second region as claimed. However, the purpose of the isolation trench by Hunter et al has clearly been stated to include trench isolation for suppressing latch-up in CMOS devices (cf. col. 1, lines 12-28); therefore, an obvious application of the isolation trench by Hunter et al is to the CMOS device structure of Figure 1 in Yamaguchi et al in which the central trench separates NMOS and PMOS devices, the NMOS device being on the side of the said first region, while the second region is the N+ region biased, in fact: connected, to Vss, while said first region is biased by the gate electrode of the PMOS device. Hence it is seen that the not specifically claimed limitations by Hunter et al are present in an obvious application of the kind for which Hunter et al intended their trench isolation invention.

Motivation to include said teaching by Yamaguchi et al is provided by the intended application by Hunter et al to deep trench isolation of CMOS devices (inter alia) as stated in their "Background", for the purpose of latch-up suppression (cf. col. 1, line 24). *Combination* of said teaching with said invention is straightforward because at

most the trench already shown by Yamaguchi et al would have to dug a little more deeply into the P+ substrate. *Success* of the implementation of said combination can therefore be reasonably expected.

On claim 18: said isolating element 36 comprises a dielectric material (oxide layer 38) (cf. col. 3, lines 40-45).

On claim 19: said isolating element 36 further comprises polycrystalline silicon (cf. col. 3, lines 55-62).

On claim 20: the device of claim 18 as taught by Hunter et al and Yamaguchi et al has p-type for the first conductivity type (see discussion of claims 12 and 17).

7. ***Claim 21*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al and Yamaguchi et al as applied to claim 17 above, and further in view of Mavencamp (6,175,277). Although Hunter et al and Yamaguchi do not necessarily teach the further limitation as defined by claim 21, application of the device by Hunter et al and Yamaguchi et al, i.e., a CMOS device with latchup protection, to power transistors is an obvious application of the invention, as evidenced from Mavencamp, who teaches CMOS power transistors (see, for instance, claim 1 by Mavencamp), while it is understood in the art that latchup is a ubiquitous concern for CMOS devices. Claim 21 thus merely recites an obvious application of the invention.

8. ***Claims 22-25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE J. Solid-State Circuits, Vol. sc-20 (1), February 1985) and Nakagawa (6,239465 B1).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines 21-63) positioned on one side of said first region and extending from the surface of said epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al nor Yamaguchi et al necessarily teach the further limitation that said isolating element should have "a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and second regions". However, Nakagawa teaches isolation trenches for prevention of electrical interference between different superficial portions of the device and with a length substantially equal to the width of the chip (cf.

Figures 5 and 8) and such that each of said portions include said first and second regions (numeral 28 in Nakagawa; see also Figure 3 in Nakagawa).

Motivation to include the teaching by Nakagawa in the invention of Hunter et al and Yamaguchi et al is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in the device by Hunter et al and Yamaguchi et al not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Hunter et al and Yamaguchi et al in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as taught by Hunter et al and Yamaguchi et al.

On claims 23-25: said isolating element by Hunter et al and Yamaguchi comprises a dielectric material 38 (cf. col. 3, lines 37-45 in Hunter et al) (*claim 23*) and also comprises polycrystalline silicon 42 (cf. col. 3, lines 55-62 in Hunter et al) (*claim 24*), while the first conductivity type is p-type (*claim 25*) (see above, discussion of claim 22).

9. ***Claim 26*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al, Yamaguchi et al and Nakagawa as applied to claim 22 above, and further in view of Mavencamp (6,175,277 B1). Although Hunter et al nor Yamaguchi nor Nakagawa necessarily teach the further limitation as defined by claim 26, application of the device

by Hunter et al, Yamaguchi et al and Nakagawa, i.e., a CMOS device with latchup protection, to power transistors is an obvious application of the invention, as evidenced from Mavencamp, who teaches CMOS power transistors (see, for instance, claim 1 by Mavencamp), while it is understood in the art that latchup is a ubiquitous concern for CMOS devices. Claim 26 thus merely recites an obvious application of the invention.

Double Patenting

10. Claim 19 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 13. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). In particular, first and second regions as claimed as completely interchangeable, and hence there is no difference between claim 13 and claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
June 1, 2003